Remarks

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1-6 are amended. Claims 7-9 are added. Claims 1-9 are pending in the application.

I. Objection to the Claims

Claim 6 was objected to. In light of the comments noted in the outstanding Office Action, claim 6 was amended. Accordingly, it is respectfully requested that this objection be withdrawn.

II. Rejection under 35 U.S.C. § 102

In the Office Action, at page 2, numbered paragraph 4, claims 1-6 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,524,217 to Sone et al.

Claim 1

This rejection is respectfully traversed because Sone does not discuss or suggest an "output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system, " a "switching control means for switching an output state of said output means, " and "an assert mechanism that maintains the wired OR signal line in an asserted state in response to an asserted state transferred by the output means of the other system," as recited in independent claim 1.

As a non-limiting example, the present invention, as recited in claims 1-6, is a device that allows for transmission of a wired OR signal between two systems. A first wired OR signal line in the first system is asserted to a low level by a first system side device, and this asserted state is transferred to the second system, where a second wired OR signal line is asserted. After the device that asserts the first signal line to a low level is processed, values in registers are changed from a predetermined value, and thereafter, the first system outputs and transfers a negate state to the second system. The second signal line is then no longer asserted, and the second signal line maintains the negate state. Thereafter, the negate state is transferred to the first system, causing the first signal line to be being asserted.

Sone discusses enabling wired-OR signal lines to be connected without interlock. In Sone:

> when a particular peripheral device (an adapter) requests an interrupt for an MPU, the -IRQn line assigned to the peripheral device is driven to its low (low voltage level) state (A)...[and] on termination of the interrupt processing routine, the MPU makes notification of the end of interrupt (EOI) to the adapter of the peripheral device so that to drive the -IRQn line to its high (high voltage level) state (D) (col. 10, lines 39-50).

Sone does not discuss or suggest an output means that outputs one of the signal or negate states from the first system to the other system and that the output state of the output means is switched by a switching control means. Sone merely discusses that:

> to represent the level of a -IRQn line of the secondary system by the shadow register 46 of the primary system, it is necessary to send an IRQ packet from the secondary system to the primary system whenever the level of the -IRQn line of the secondary system is toggled (col. 11, lines 17-21).

Sone discusses sending an IRQ packet so that the shadow register of the other system reflects the toggled state of the first system. Specifically in the lines cited by the Examiner, Sone makes no mention of an output means that switches between a first state and a second state of the wired OR signal line and outputs either state *to the other system*, and a switching control means that switches that output state of the output means. Col. 13, lines 44-67 discuss that an IRQ packet is sent or not if the primary -IRQn line is toggled from the high state to the low state depending on whether the secondary -IRQn line is asserted or not. If the primary shadow register indicates that the secondary line is not asserted, an IRQ packet is sent. If the primary shadow register indicates that the secondary line is asserted, the sending of an IRQ packet is inhibited, even if the primary -IRQn line is asserted. Then,

> the shadow register [of the receiver of the IRQ processor in the secondary system] is toggled to toggle the IRQn line to assertion or negation in response to an IRQ packet sent from the [other] system unless the primary requesting flag indicates a requesting state (col. 14, lines 14-18).

Sone merely provides that an IRQ packet is sent to the other system when it is necessary to toggle the IRQn line of the other system, but does not discuss or suggest that the switching control means switches the output state of the output means in the *first* system. The present invention, in contrast, provides that when the value in the first register of the first system changes from a predetermined value, the mask mechanism of the first system outputs the negate state (after the first wired OR signal line is maintained in an asserted state) and transfers

this outputted negate state to the second system, which causes the assert mechanism of the second system to stop asserting the second wired OR signal line (p. 14, lines 1-11).

Further, Sone only discusses that this transferred state occurs on the side of the secondary system, based on whether the registers of the secondary system indicate a high or low state. In the lines cited by the Examiner that allegedly correspond to the switching control means (col. 12, lines 16-38):

> [once] the wired-OR type -IRQn line goes high as the adapter toggles the -IRQn line from the low state to the high state,...an IRQ packet is sent from the primary system to the secondary system...so that the secondary register is toggled from the low indication state to the high indication state. [Then] the secondary -IRQn line is turned from the low indication state to the high indication state in response to the toggle of the secondary shadow register.

Sone does not discuss or suggest that a switching control means in one system switches the output state of output means of that system which is thereafter output to the other system, as discussed in independent claim 1. In Sone, when the secondary register is toggled from the low state to the high state, the secondary system returns an ACK to the primary system, which toggles the primary shadow-shadow register. The primary shadow-shadow register merely operates as a mirror image of the secondary shadow register (col. 11, lines 44-47).

Additionally, Sone does not discuss or suggest "an assert mechanism that maintains the wired OR signal line in an asserted state in response to an asserted state transferred by the output means of the other system." The assert mechanism alleged by the Examiner in col. 14, lines 1-18 discusses that assertion or negation is determined and:

> the shadow register (of the primary system) is toggled to toggle the IRQn line to assertion or negation in response to an IRQ packet sent from the secondary system unless the primary requesting flag indicates a requesting state (col. 14, lines 6-13).

Sone does not discuss or suggest that an assert mechanism is used to maintain the wired OR line in an asserted state in response to the asserted state transferred by the output means of the other system. Sone makes no mention of an assert mechanism that maintains the asserted state *in response to* an asserted state transferred by the output means of the other system.

Therefore, as Sone does not discuss or suggest an "output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system, " a "switching control means for switching an output state of said

output means, " or "an assert mechanism that maintains the wired OR signal line in an asserted state in response to an asserted state transferred by the output means of the other system," as recited in independent claim 1, claim 1 patentably distinguishes over the reference relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claim 2

Claim 2 depends from claim 1 and includes all the features of that claim, plus additional features that are not discussed or suggested by the reference relied upon. For example, claim 2 recites that "said switching control means comprises a register controlled by a processor in the system, and output means comprises: a mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value; and a transmission mechanism that transfers an output from said mask mechanism to the other system." Therefore, claim 2 patentably distinguishes over the reference relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claim 3

In regard to claim 3, Sone does not discuss or suggest "a switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state," "switching and controlling means for switching the output of said switching and outputting means," and "an assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means," as recited in independent claim 3. The Examiner alleges that col. 13, lines 44-56 correspond to the switching and outputting means of the present invention, col. 12, lines 16-38 correspond to the switching and controlling means, and col. 14, lines 1-18 correspond to the assert mechanism.

First, the cited section in Sone does not discuss or suggest a switching and outputting means for switching between a first state transmitted by the output means in the other system and a second state where negate state is output and outputting the switched state. Sone merely discusses at col. 13, lines 44-56 that:

> the IRQn line 51 is toggled from the high (high voltage level) state to the low (low voltage level) state... [and] if the shadow register is set to 0 (high indication state)... a request to send a packet is made from the IRQ prioritizer 48....

The cited sections in Sone do not discuss a switching and outputting means for switching between the first state transmitted *by the output means of the other system* and a second state where negate state is output. Sone makes no indication that there is switching (in the second system) between the first state where the signal state transmitted by the other system is output and a second state where negate state is output and then outputting the switched state. Sone only discusses that the IRQn line is toggled based on whether the shadow register of that system is toggled and that the shadow register is toggled when an IRQ packet is sent from the first system.

Further, Sone does not discuss or suggest a "switching and controlling means for switching the output of said switching and outputting means," where the switching and outputting means switches between a state transmitted by the output means of the other system and a second state where negate state is output. The Examiner alleges that col. 12, lines 16-38 correspond to the "switching and controlling means," however, the cited lines merely make reference to the primary IRQn line being returned from a low state to the high state, the secondary register being toggled to the high indication state and the secondary -IRQn line being turned from the low indication state to the high indication state. Sone further discusses that, as the primary shadow register is in the high indication state, "no IRQ packet is sent to the primary system in response to the toggle of the secondary -IRQn line" (col. 12, lines 35-38). As discussed above with respect to the "switching control means" of claim 1, Sone does not discuss switching the output of the switching and outputting means, where the switching and outputting means switches between the first state where the signal state transmitted by the output means in the other system is output and the second state. Sone does not discuss or suggest that a switching and controlling means switches the output of the switching and outputting means of the same system, where the switching and outputting means switches between a first state transmitted by the other system and a second state.

Additionally, Sone does not discuss or suggest an assert mechanism that switches the wired OR signal line between an asserted and negate state according to the output state of the switching and outputting means. Again, Sone does not discuss or suggest that there is an assert mechanism of one system that switches the signal line between an asserted state or a negate state *according to the output state* of the switching and outputting means, where the switching and outputting means switches between a first state transmitted by the output means of the other system is output and a second state.

Therefore, as Sone does not discuss or suggest "a switching and outputting means for

switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state," "switching and controlling means for switching the output of said switching and outputting means," or "an assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means," as recited in independent claim 3, claim 3 patentably distinguishes over the reference relied upon.

Claim 4

Claim 4 depends from claim 3 and includes all the features of that claim, plus additional features that are not discussed or suggested by the reference relied upon. For example, claim 4 recites that "said switching and controlling means is composed of a register controlled by a processor in the system, and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value other than the predetermined value." Therefore, claim 4 patentably distinguishes over the reference relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claims 5 and 6

As to independent claims 5 and 6, Sone does not discuss or suggest "switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state; processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and switching each of said output means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said output means to the first state, after finishing the processing of the device," as recited in independent claim 5 and similarly in independent claim 6.

As cited in the Office Action, "processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching" corresponds to col. 10, lines 33 to col. 11, line 4. Col. 10, lines 33 to col. 11, line 4 discuss that when the peripheral device requests an interrupt, the -IRQn line is driven to the low state, then returns to the high state. However, Sone does not discuss or suggest the processing of a device that has brought the wired OR signal line in the *other* system into the asserted state, after the switching is done. Further, Sone does not discuss or suggest switching the output means of both systems to the

second state, verifying the negate system in the two systems, then switching each of the output means to the first state, after finishing the processing of the device from the other system. Sone discusses that the -IRQn line assigned to that device is driven to its low state and then on termination of the interrupt processing routine, the peripheral device drives the -IRQn line to its high state. Sone does not discuss that, after the switching, the device of the other system is processed and thereafter, each of the output means are switched to the second state. Sone does not discuss that the negate state of the wired OR signal lines in the two systems is verified and then each of the output means is switched to the first state after the processing of the device is finished. In the present invention:

> ...the first and second wired OR signal lines are asserted to the low level..., and a device different from the one having already made an assertion subsequently asserts the wired OR signal. In this case, even if the processor has finished processing the first asserting device and the values in the first and second registers are changed to mask outputs from the first and second mask mechanisms to establish the negate state, the first or second wired OR signal to which the second asserting device is connected is maintained in the asserted state. Then, the processor executes processing of the second asserting device...[which] stops the assertion made by the second asserting device,...[and the processor verifies] that the wired OR signal has been negated. After the verification, the processor returns the values in the first and second registers to the predetermined value that precludes outputs from the first and second mask mechanisms, respectively, from being masked" (page 15 line 11-page 16, line 9).

Sone does not discuss or suggest that, after the processing of the device, each of the output means is switched to the first state.

Further, the acknowledgment, cited by the Examiner to correspond to verification of the negate state, that is sent from one system to the other is merely used to toggle the shadow-shadow register of the other system so that the shadow-shadow register of the other system operates as a mirror image of the shadow register of the first system. The acknowledgement makes no such verification of a negate state.

Therefore, as Sone does not discuss or suggest "switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state; processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and switching each of said output means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said output means to the first state, after finishing the processing of the device," as recited in claim 5,

and similarly in claim 6, claims 5 and 6 patentably distinguish over the reference relied upon.

III. New Claims

New claim 7 recites that the features of the present invention include "causing the asserted state of the first signal line to be transferred to a second wired signal line of a second system, which transfers the asserted state of the second line to the first line, thereby maintaining the asserted states of the first and the second wired signal lines after the first system device is turned off to stop asserting the first wired signal line." Nothing in the reference relied upon discusses or suggests such. It is submitted that new claim 7 distinguishes over the reference relied upon.

New claim 8 depends from claim 7 and includes all the features of claim 7, plus additional features that are not discussed or suggested by the reference relied upon. For example, claim 8 recites "changing a value in a first register in the first system from a predetermined value; and transferring a negate state from the first system to the second system, based on the change from the predetermined value; wherein the second wired signal line is thereafter not asserted." Nothing in the reference relied upon discusses or suggests such. It is submitted that new claim 8 distinguishes over the reference relied upon.

New claim 9 recites that the features of the present invention include that "if a value in the register changes from a predetermined value, a negate state is output and transferred from the first system to the second system so the first wired signal line and the second wired signal line are brought into a negate state." Nothing in the reference relied upon discusses or suggests such. It is submitted that new claim 9 distinguishes over the reference relied upon.

Conclusion

In accordance with the foregoing, claims 1-6 have been amended. Claims 7-9 have been added. Claims 1-9 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 4/5/06

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